SX3 HDMI 4K Capture Kit

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Drawing Numbers	
PCBA	121-60612-01
PCB	600-60612-01
FAB DRW	610-60612-01
ASSY DRW	620-60612-01
SCH DRW	630-60612-01

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SCH Title : SX3 HDMI 4K Capture Kit

Page Title : Title Page

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A4	630-60612-01	MISHRASANATK	RAJA	04

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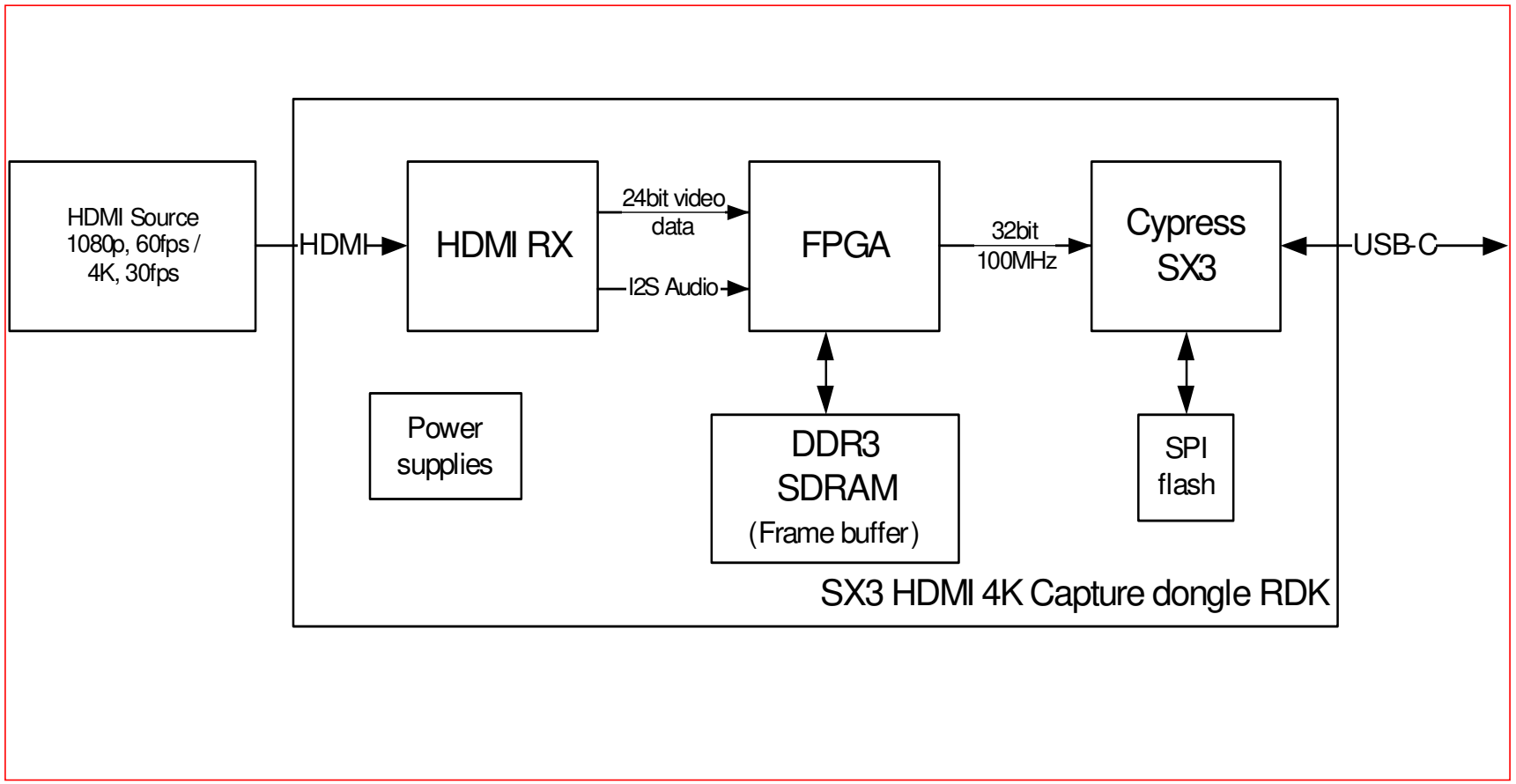

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Page Title : Block diagram

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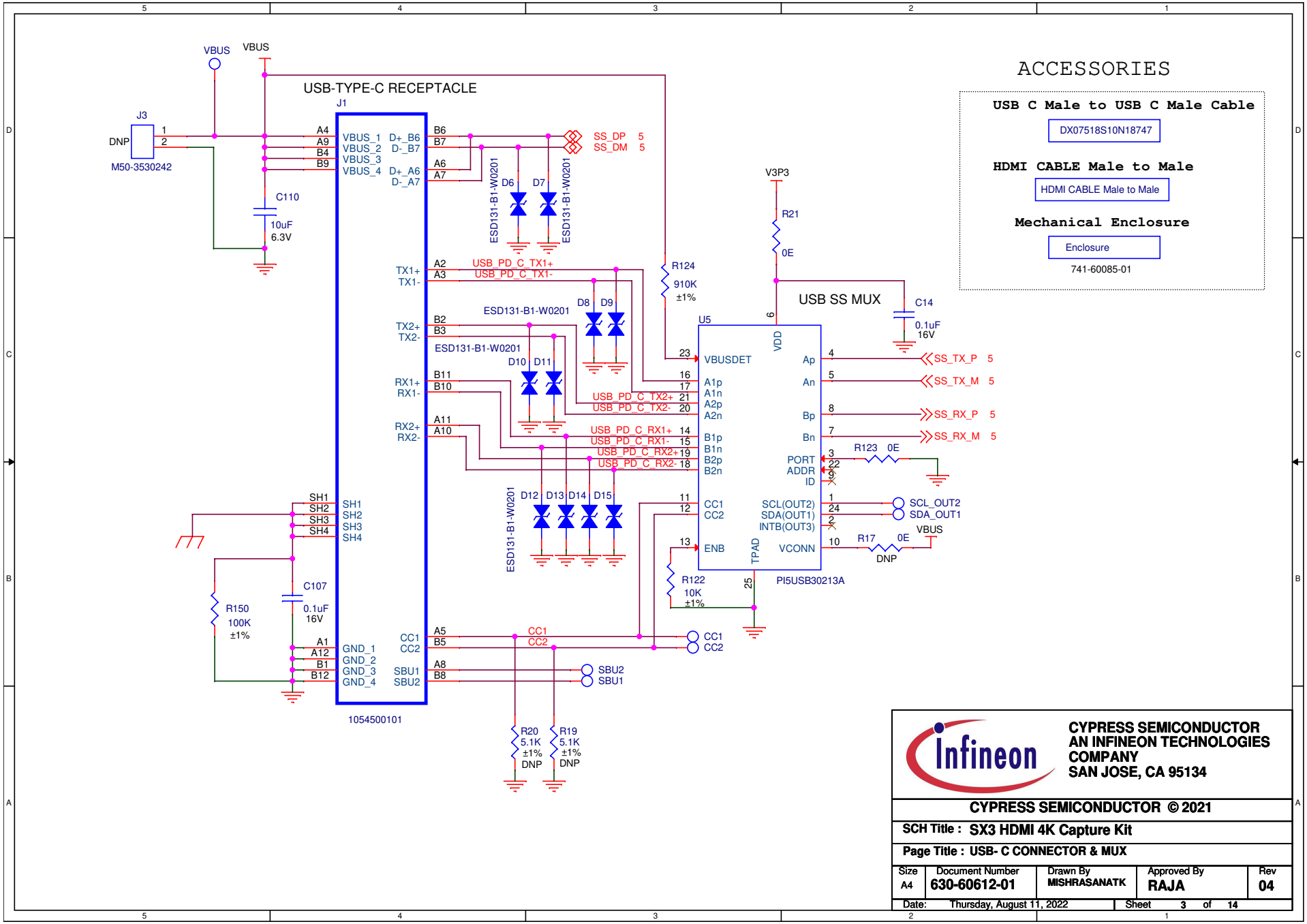

ACCESSORIES

USB C Male to USB C Male Cable

DX07518S10N18747

HDMI CABLE Male to Male

HDMI CABLE Male to Male

Mechanical Enclosure

Enclosure

741-60085-01

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SCH Title : SX3 HDMI 4K Capture Kit				
Page Title : USB- C CONNECTOR & MUX				
Size: A4	Document Number: 630-60612-01	Drawn By: MISHRASANATK	Approved By: RAJA	Rev: 04
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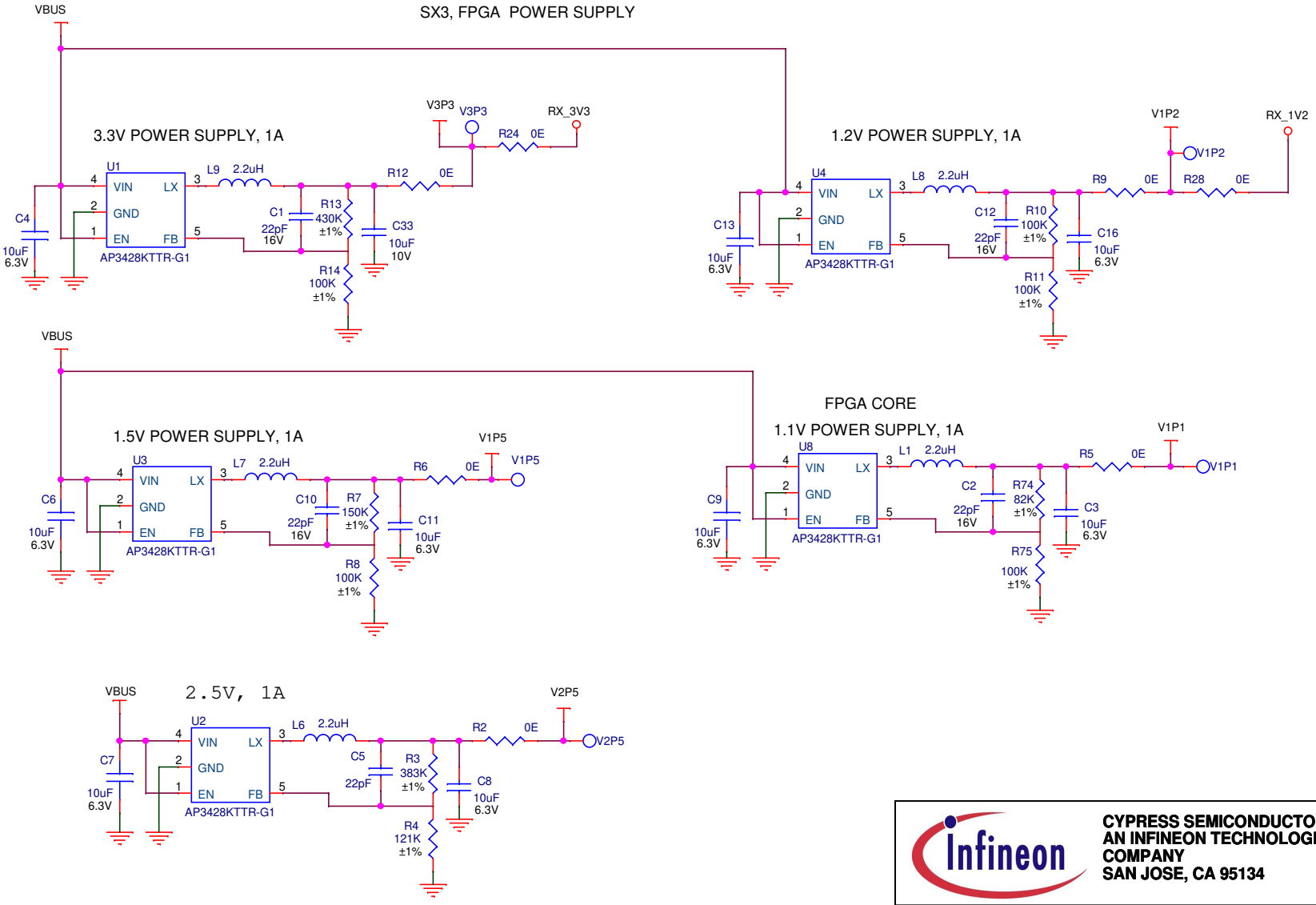

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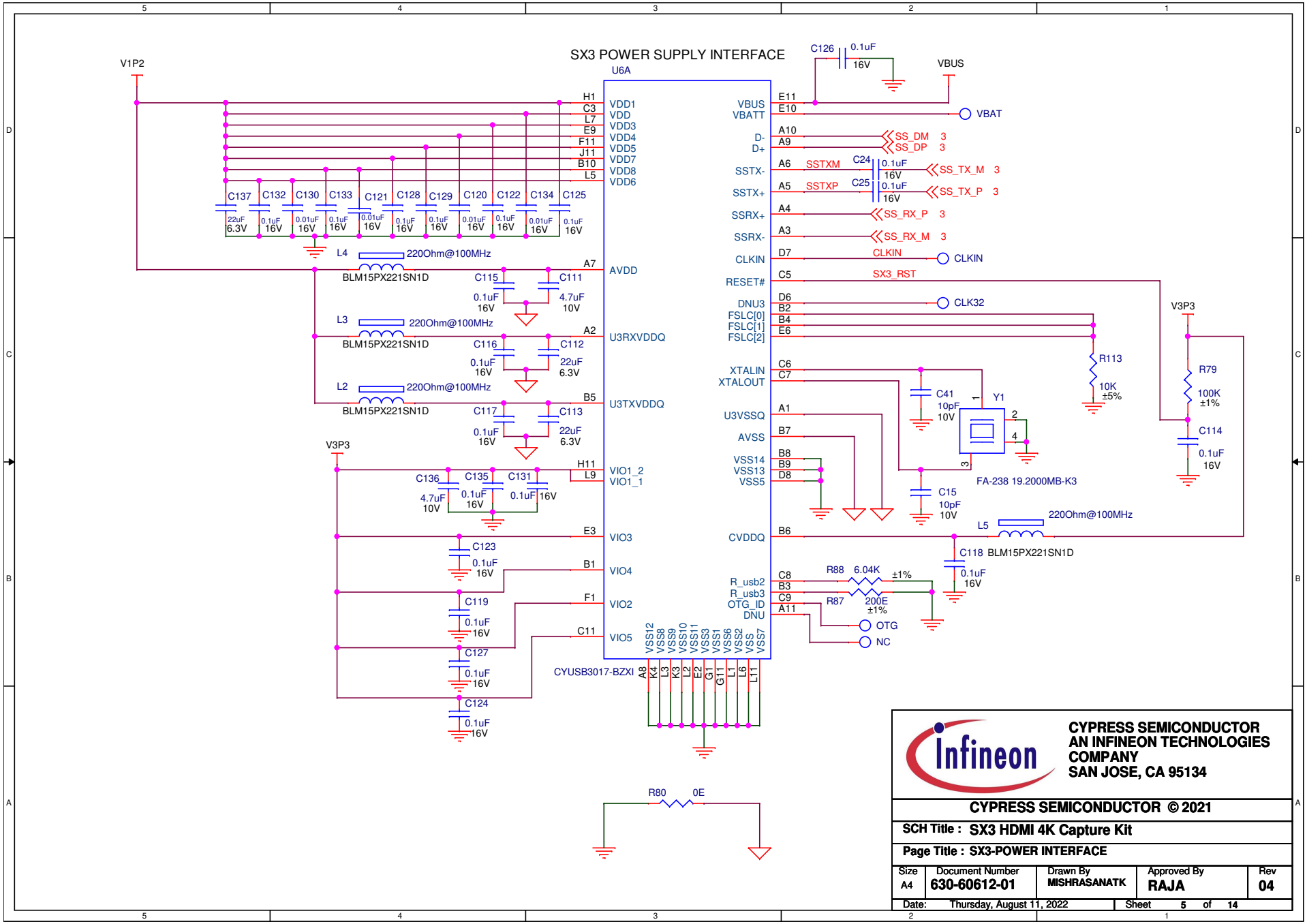
SCH Title : SX3 HDMI 4K Capture Kit				
Page Title : SX3,FPGA-POWER SUPPLY				
Size: A4	Document Number: 630-60612-01	Drawn By: MISHRASANATK	Approved By: RAJA	Rev: 04
Date: Thursday, August 11, 2022		Sheet 4 of 14		


SX3 POWER SUPPLY INTERFACE
U6A
V1P2
VBUS
VBAT
CLKIN
CLK32
SX3_RST
SS_DM 3
SS_DP 3
SS_TX_M 3
SS_TX_P 3
SS_RX_P 3
SS_RX_M 3
SSTXM
SSTXP
V3P3
FA-238 19.2000MB-K3
CYUSB3017-BZXI
OTG
NC
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Document Number 630-60612-01
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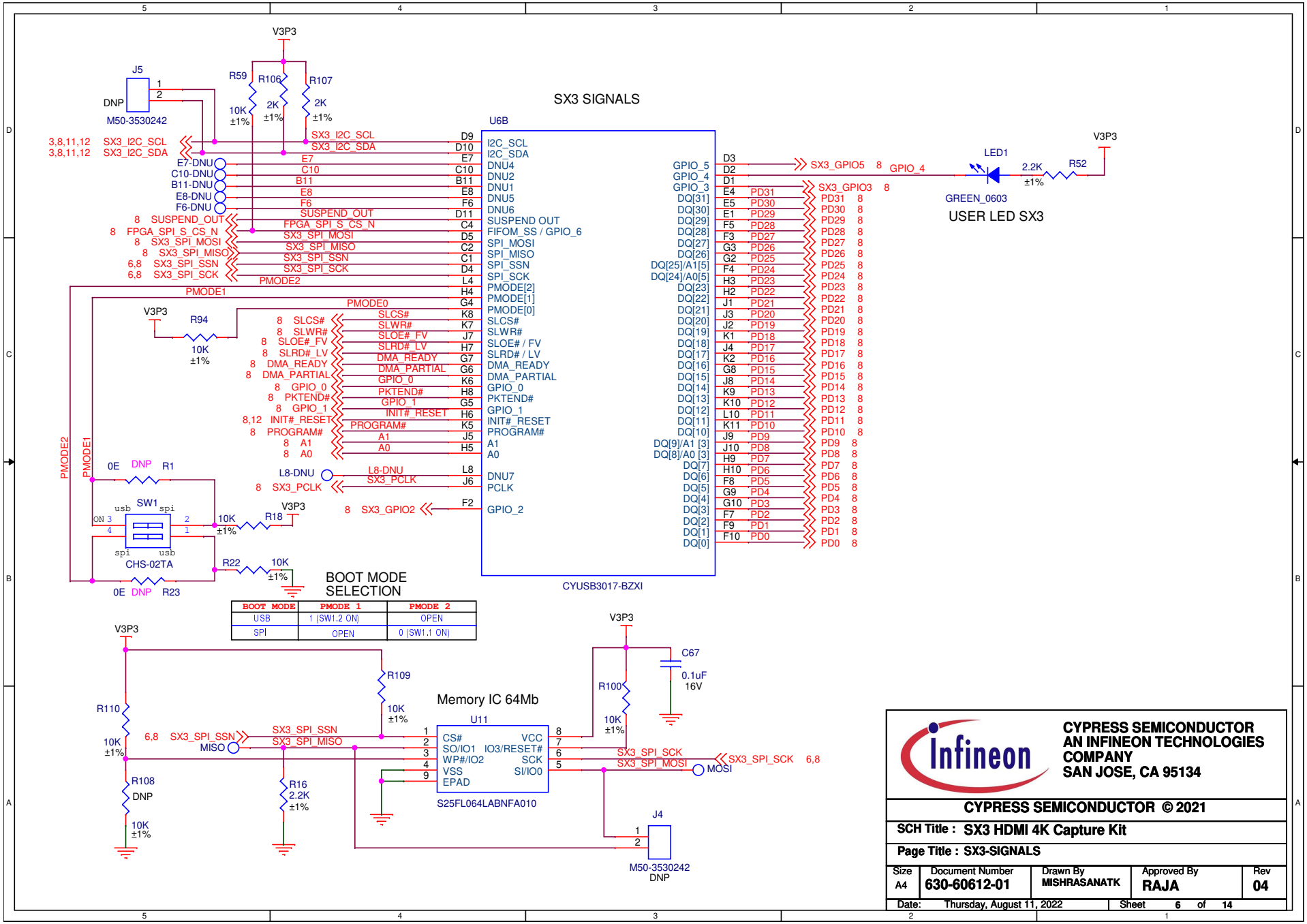
SX3 SIGNALS
U6B
CYUSB3017-BZXI
USER LED SX3
LED1
GREEN_0603
J5
M50-3530242
SW1
CHS-02TA
BOOT MODE SELECTION
BOOT MODE | PMODE 1 | PMODE 2
USB | 1 (SW1.2 ON) | OPEN
SPI | OPEN | 0 (SW1.1 ON)
Memory IC 64Mb
U11
S25FL064LABNFA010
J4
M50-3530242
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Size A4
Document Number 630-60612-01
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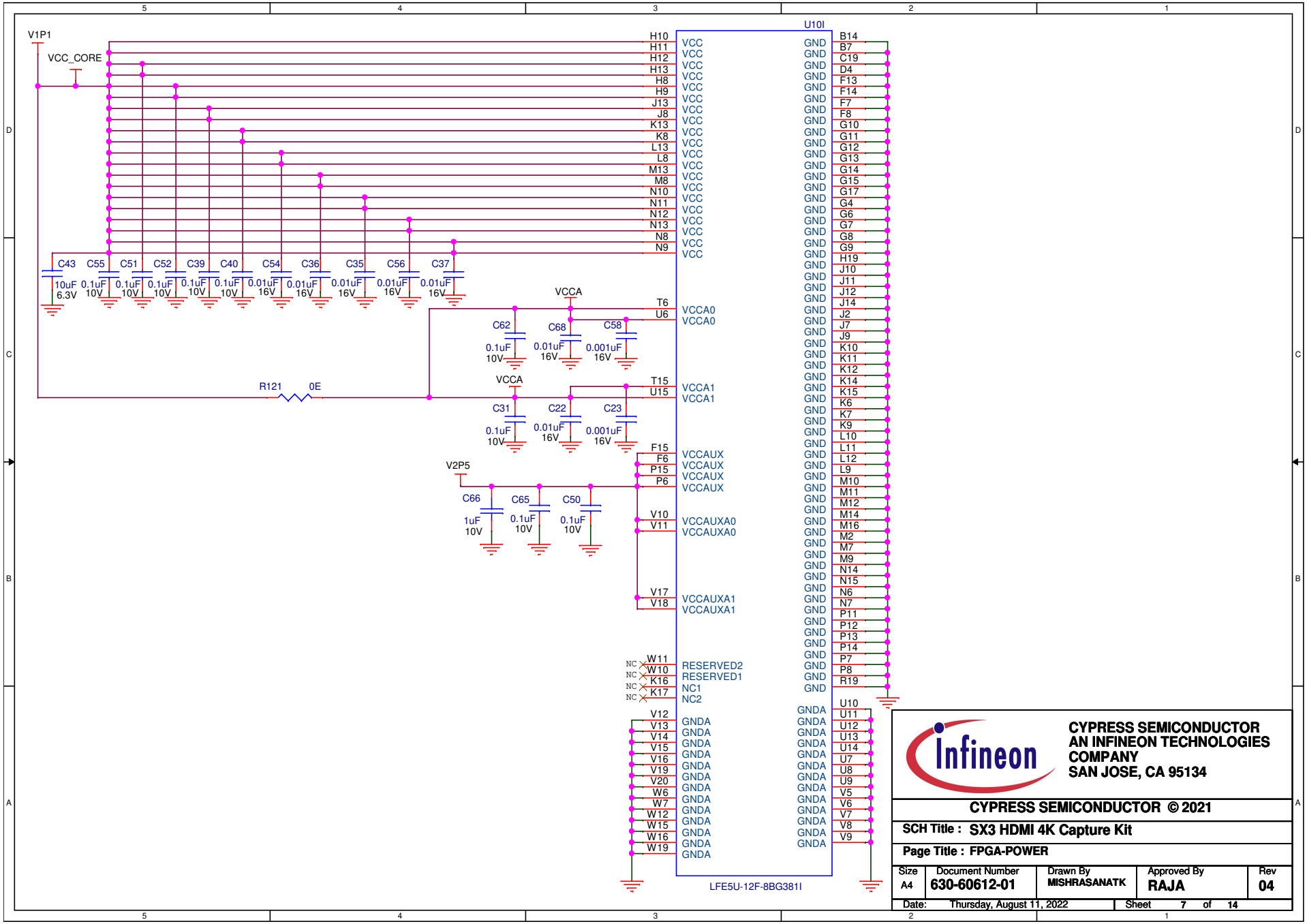
V1P1
VCC_CORE
U10I
LFE5U-12F-8BG381I
C43 10uF 6.3V
C55 C51 C52 C39 C40 0.1uF 10V
C54 C36 C35 C56 C37 0.01uF 16V
VCCA
C62 0.1uF 10V
C68 0.01uF 16V
C58 0.001uF 16V
R121 0E
C31 0.1uF 10V
C22 0.01uF 16V
C23 0.001uF 16V
V2P5
C66 1uF 10V
C65 C50 0.1uF 10V
VCC
VCCA0
VCCA1
VCCAUX
VCCAUXA0
VCCAUXA1
RESERVED2
RESERVED1
NC1
NC2
GND
GNDA
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Page Title : FPGA-POWER
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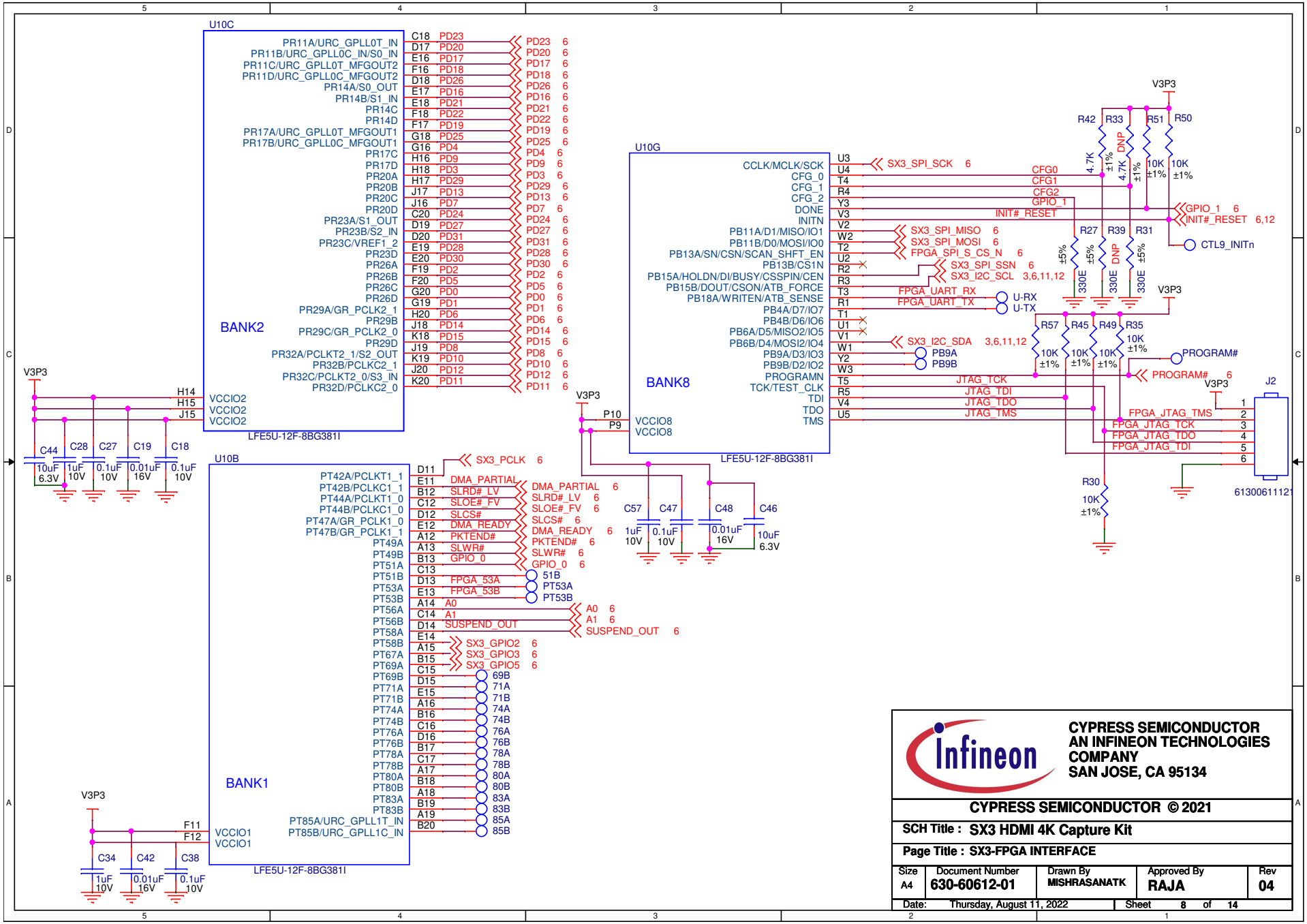
U10C
BANK2
LFE5U-12F-8BG381I
U10G
BANK8
U10B
BANK1
V3P3
J2
61300611121
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Page Title : SX3-FPGA INTERFACE
Size A4
Document Number 630-60612-01
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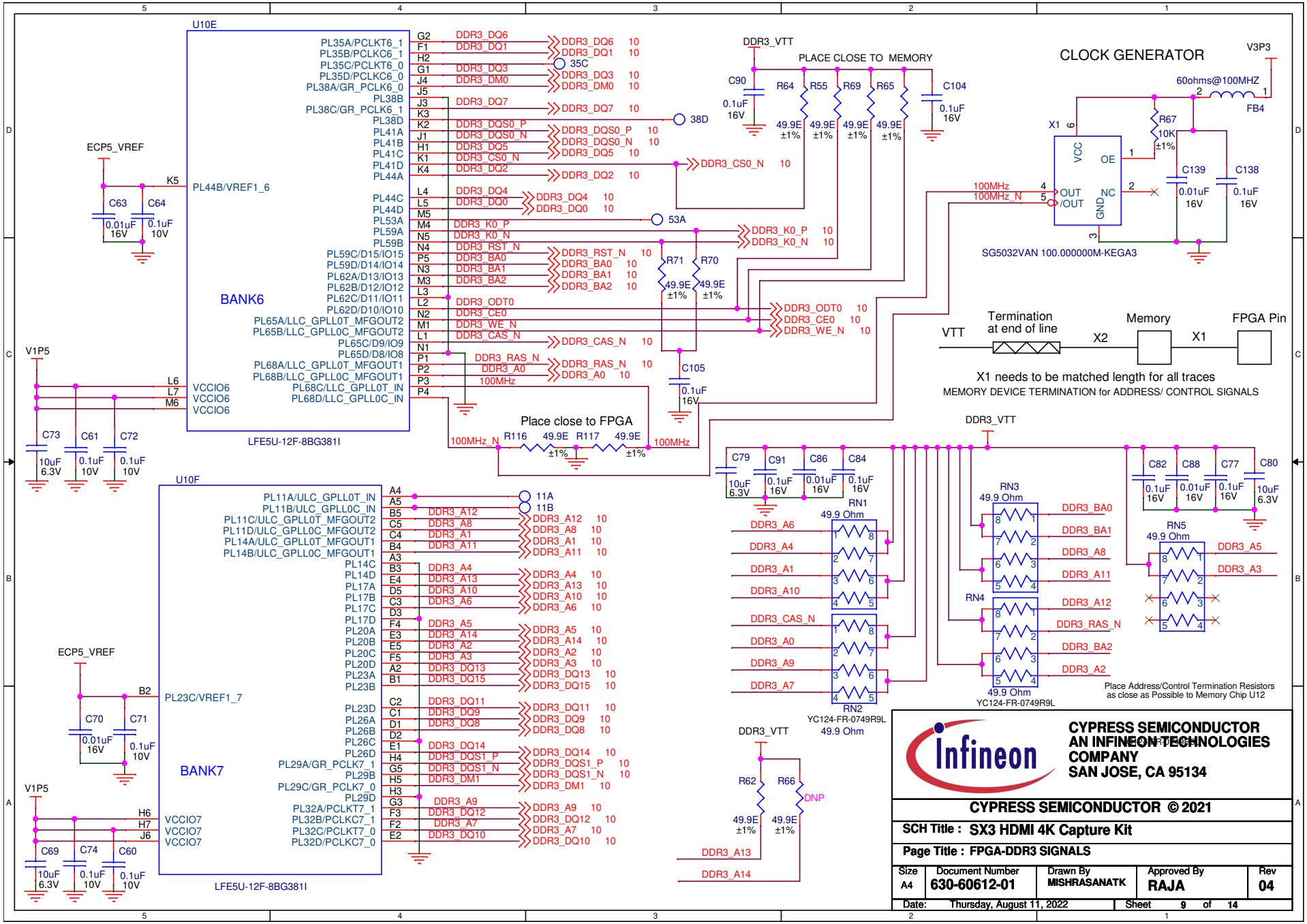
U10E
BANK6
LFE5U-12F-8BG381I
U10F
BANK7
LFE5U-12F-8BG381I
ECP5_VREF
V1P5
CLOCK GENERATOR
SG5032VAN 100.000000M-KEGA3
DDR3_VTT
PLACE CLOSE TO MEMORY
Place close to FPGA
VTT
Termination at end of line
Memory
FPGA Pin
X1 needs to be matched length for all traces
MEMORY DEVICE TERMINATION for ADDRESS/ CONTROL SIGNALS
Place Address/Control Termination Resistors as close as Possible to Memory Chip U12
YC124-FR-0749R9L
49.9 Ohm
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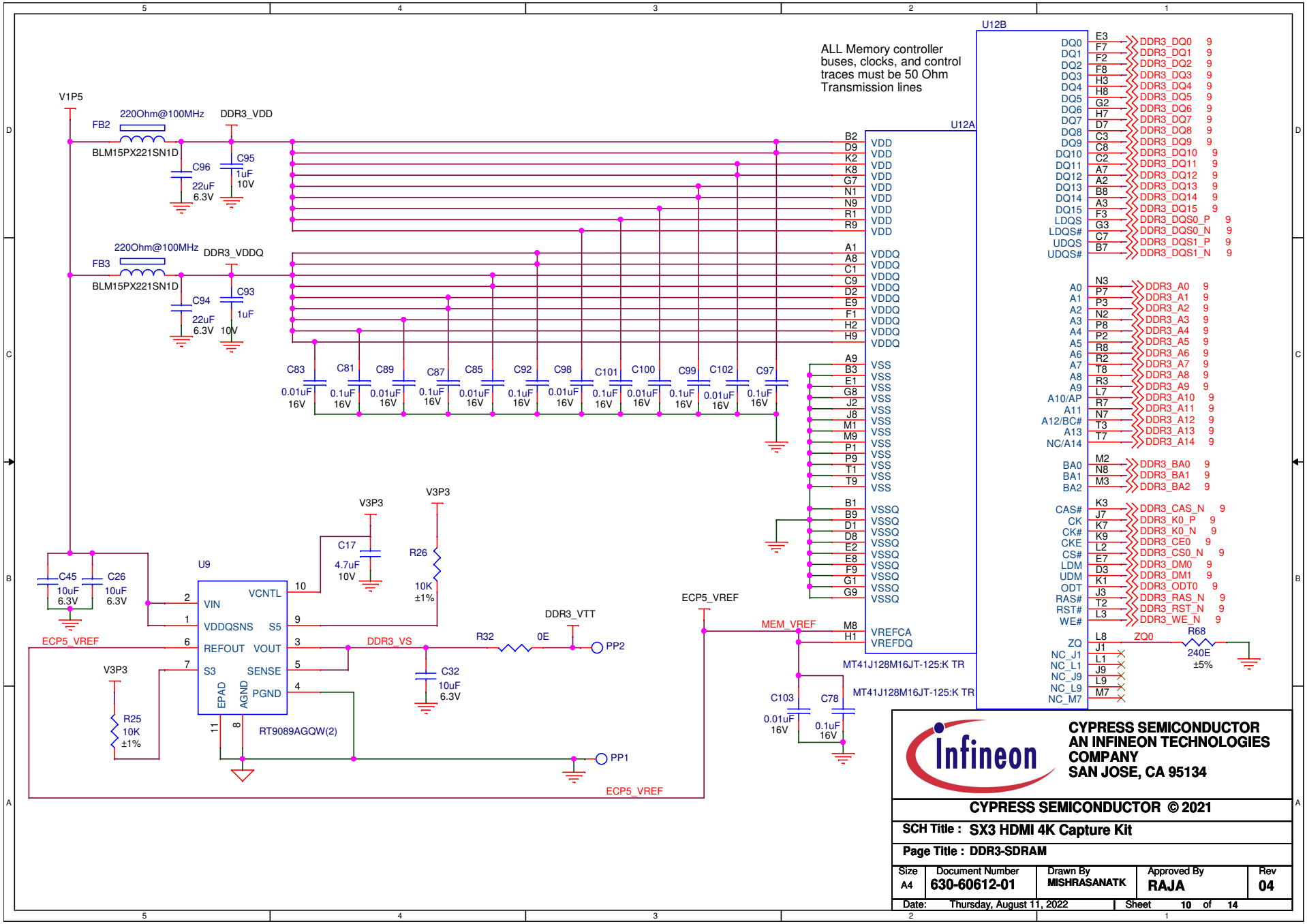

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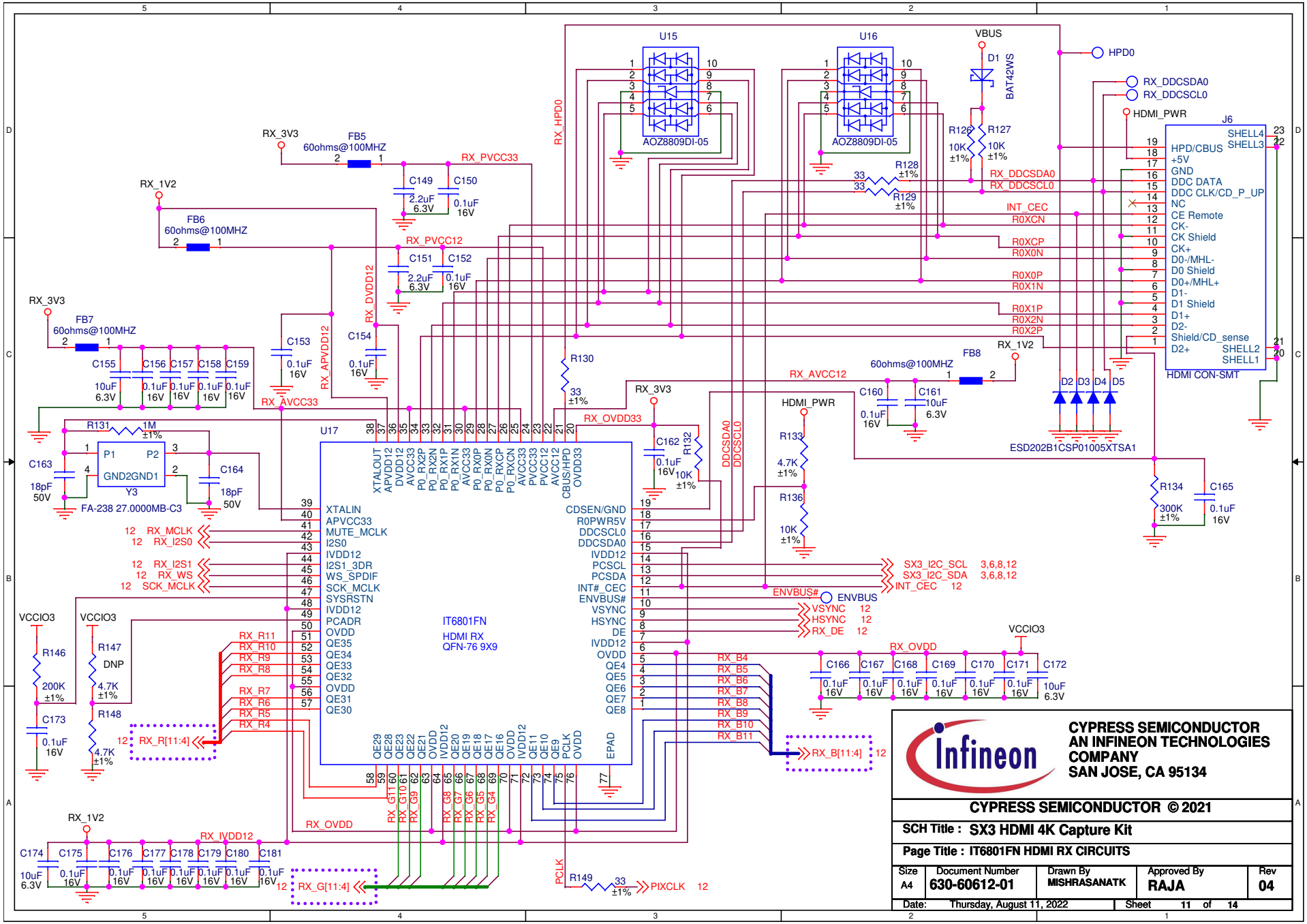

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Page Title : IT6801FN HDMI RX CIRCUITS				
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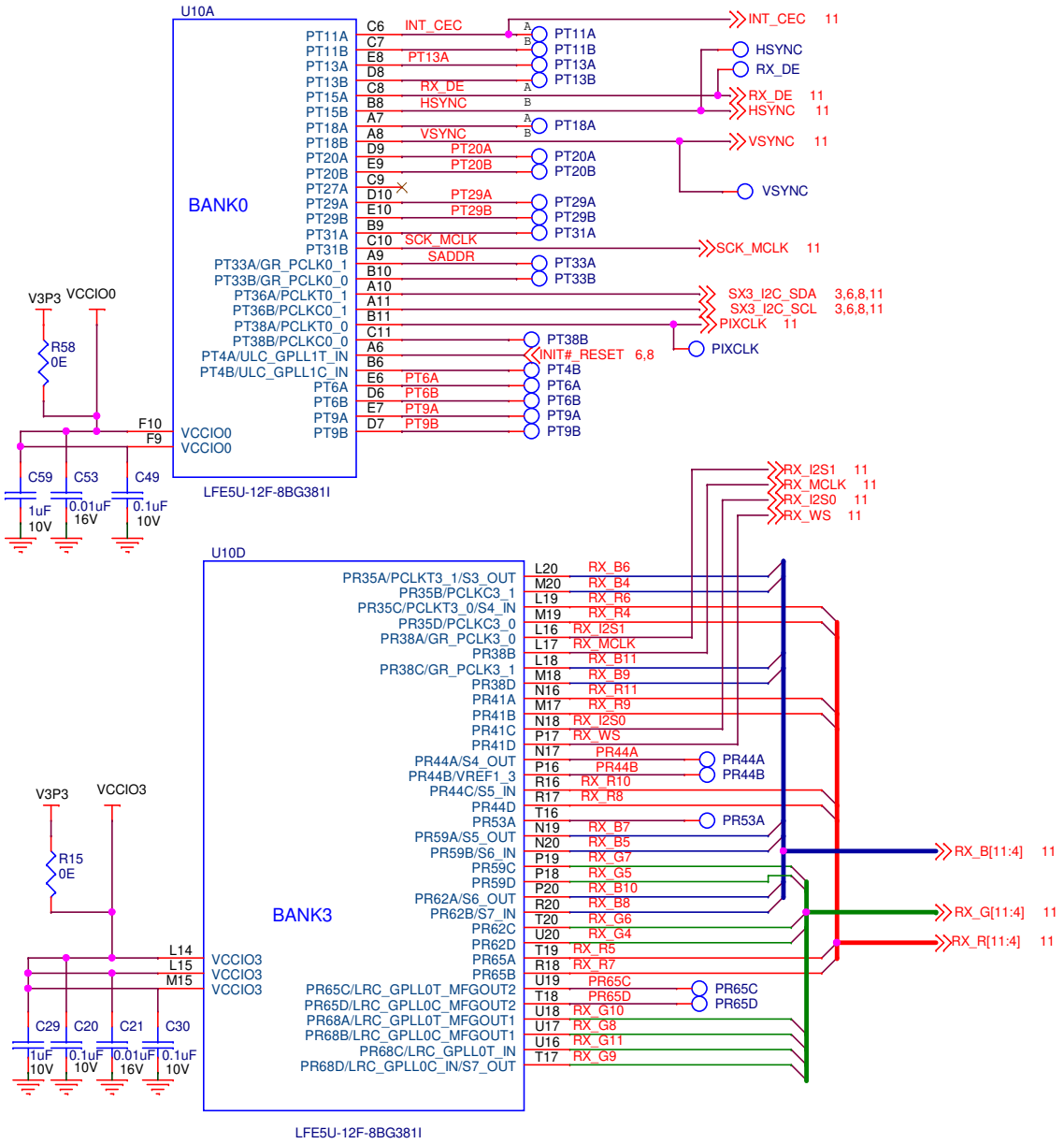
FPGA INTERFACE



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Page Title : FPGA INTERFACE & SERDES				
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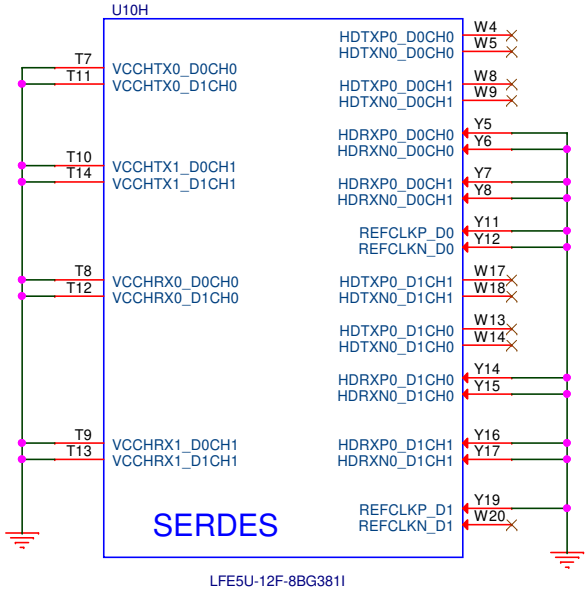

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SCH Title : SX3 HDMI 4K Capture Kit				
Page Title : FPGA-SERDES (NOT USED)				
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REVISION HISTORY

REV	DESCRIPTION OF CHANGE	DATE
01	Initial Release	13/JULY/2020
02	1.Connected V5P0_J2 to VBUS. 2.Added DIP Switch SW1 & related circuits. 3.Connected S3 and S5 to Pullup Configuration. 4.Changed J2 JTAG connector from 1.27mm pitch 7pin to 2.54mm pitch with 5 pin. 5.SX3 pin names H6,K5 were Updated as INIT#_RESET,PROGRAM# 6.Added R28 0E in series to V1P2 & RX_1V2. 7.HDMI connector CN1 ref. changed as J6. 8.INIT#_RESET updated in 6,8 and 12th page 9.J2 connector updated as 6pin connector. 10.Replacement of SPI Flash to New Part (S25FL064LABNFA010) 11.Replacement of J1 Connecter to New Part (1054500101) 12.Replacement of FPGA U10 to New Part (LFE5U-12F-8BG381C) 13.Updated USB C to C Cable with JAE part 14.Added Alternate part number (W632GU6NB-12 TR) for DDR 15. Replaced L2, L3, L4, L5, FB2, FB3 with BLM15PX221SN1D	20/JAN/2022
03	1. Populated R50. Pull up added to FPGA INITN pin	24/MAR/2022
04	1. Updated FPGA MPN to LFE5U-12F-8BG381I	20/JUL/2022

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